LCDK — 29C51/52
iATC-29C51/52 LINE CARD DEVELOPMENT KIT

- **Single Board Line Card Plus Group Controller.**
- **Minimal Assembling, Low Cost, Kit Form.**
- **Extensive System Software in ROM.**
- **Wire-Wrap Area for Custom Circuitry.**
- **A Comprehensive User's Manual.**
- **Direct Interface with a CRT Terminal.**
- **User's Manual.**

The LCDK-29C51/52 contains most of the components required for a full feature line card. The kit consists of primary and a secondary board, which with an addition of few components can be made to function as a PBX. Included is a preprogrammed ROM containing a system monitor for general software utilities and system diagnostics. The SLD LCDK-29C51/52 is designed to be operated with a dumb terminal; however, software is provided to operate the kit from an Intellec Development System. This kit is an inexpensive and highly flexible prototype system that has been designed to reduce system development time thereby leading to an increased productivity.

FUNCTIONAL DESCRIPTION

The LCDK-29C51/52 consists of two boards, namely a primary and a secondary. The kit supports up to 128 TDM timeslots and with a little additional hardware, a full feature line card. The kit as supplied, without any additional components, can be used to form a signal path between two analog sources. The LCDK comes completely assembled. The SLD LCDK-29C51/52 secondary board functional block diagram is shown in Figure 1, the primary board is a subset of the secondary.

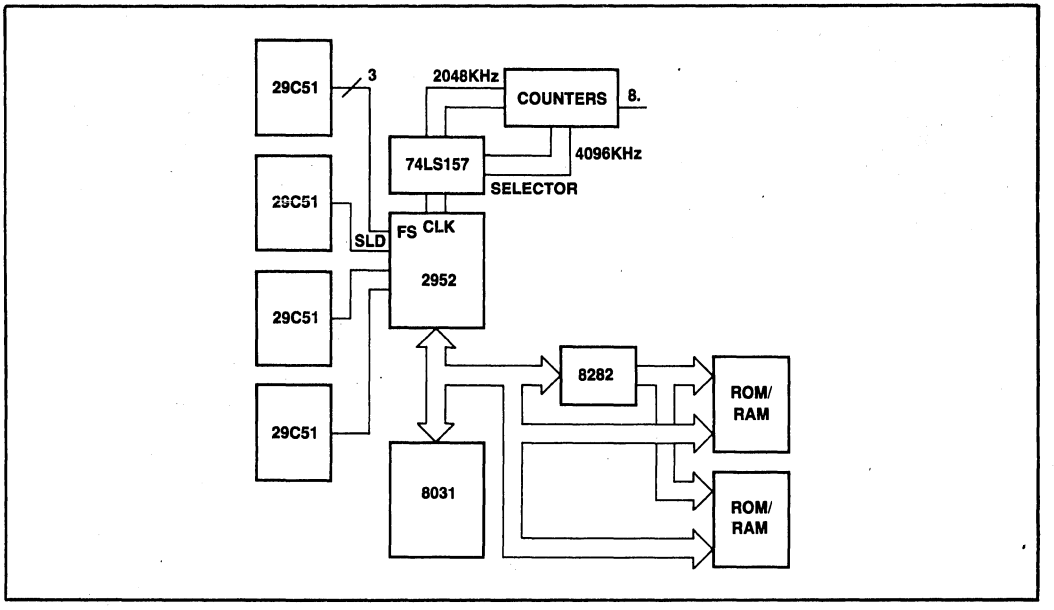

Figure 1. LCDK-29C51/52

29C51 Combo

The Intel iATC 29C51 Feature Control Combo is an advanced user-programmable, fully integrated PCM codec with transmit/receive filters fabricated in CMOS technology. The 29C51 realizes the same excellent transmission performance as the Intel 2913/2914 Combo while achieving the low power consumption typical of CMOS circuits.

The 29C51 incorporates the Supervision, Coding, Hybrid and Testing Operations out of the normal BORSCHT functions associated with an analog line interface circuit. The 29C51 also offers a secondary analog channel, programmable transmit and receive gains, on chip or custom hybrid balancing network selection and a flexible signalling interface. The 29C51 is intended for use with the 2952 Intergrated Line Card Controller in digital switching environments. A block diagram of the 29C51 Combo is shown in Figure 2.

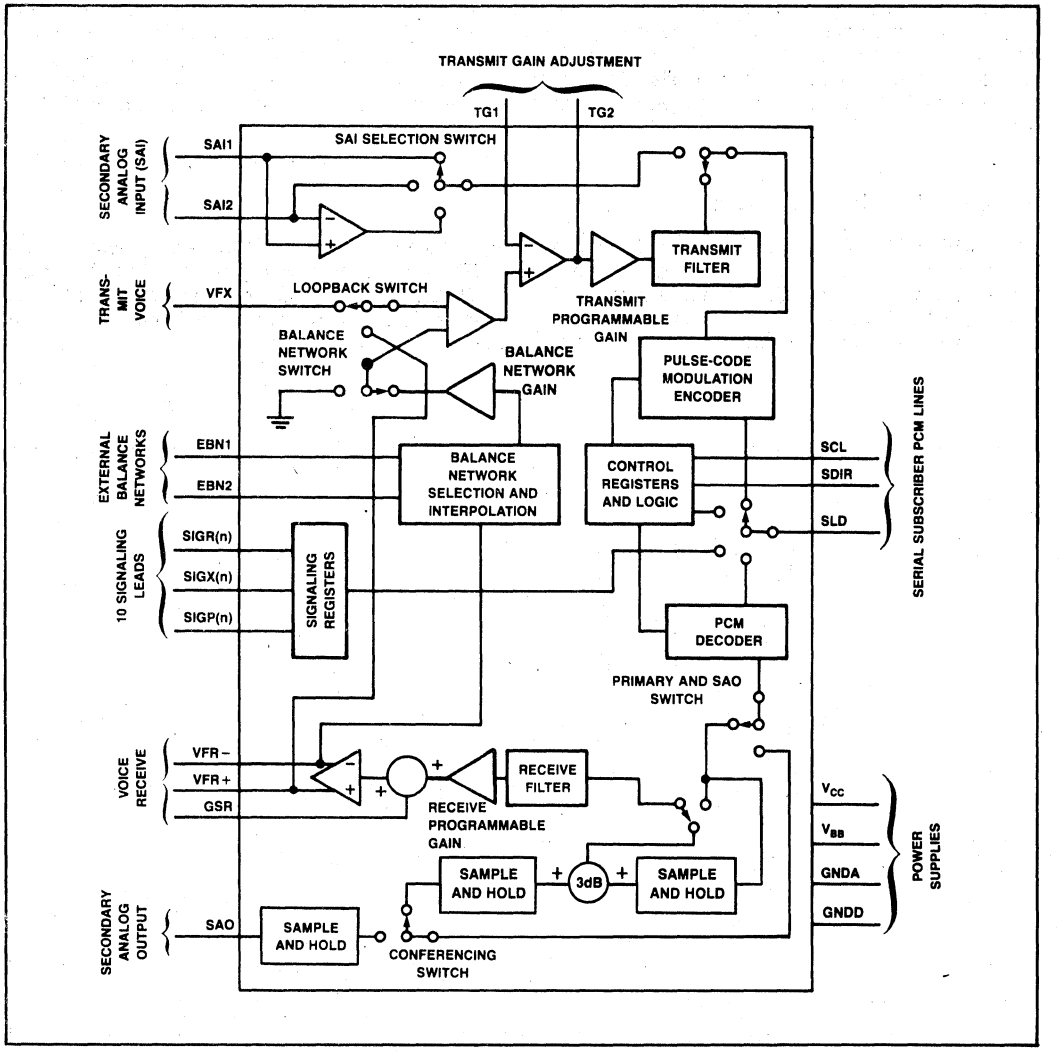

Figure 2. 29C51 Combo Block Diagram

2952 Line Card Controller

The Intel iATC 2952 Line Card Controller (LCC) is a special purpose I/O Controller optimized for use in all types of telecommunication switching systems. The 2952 replaces the traditional MSI circuits and represents the continuation of a trend to intelligent flexible line cards.

The 2952 handles the transfer of primary voice, data, feature control, and signalling information between the backplane and up to eight 29C51's; however, the LCDK-29C51/52 will only be equipped for four 29C51's per board. The 2952 and 29C51 communicate across a Subscriber Data Link (SLD) interface. The SLD is a three wire link comprising of a clock signal a serial data stream and a read/write strobe.

The 2952 is equipped with a standard microprocessor interface and independent transmit and receive DMA channels. As well as this, the 2952 has two standard PCM highways for connection to the backplane. Another feature of the 2952 is a fast serial interface to the central processor. This serial interface is intended for signalling and follows a subset of the HDLC protocol. Figure 3 shows a block diagram of the 2952.

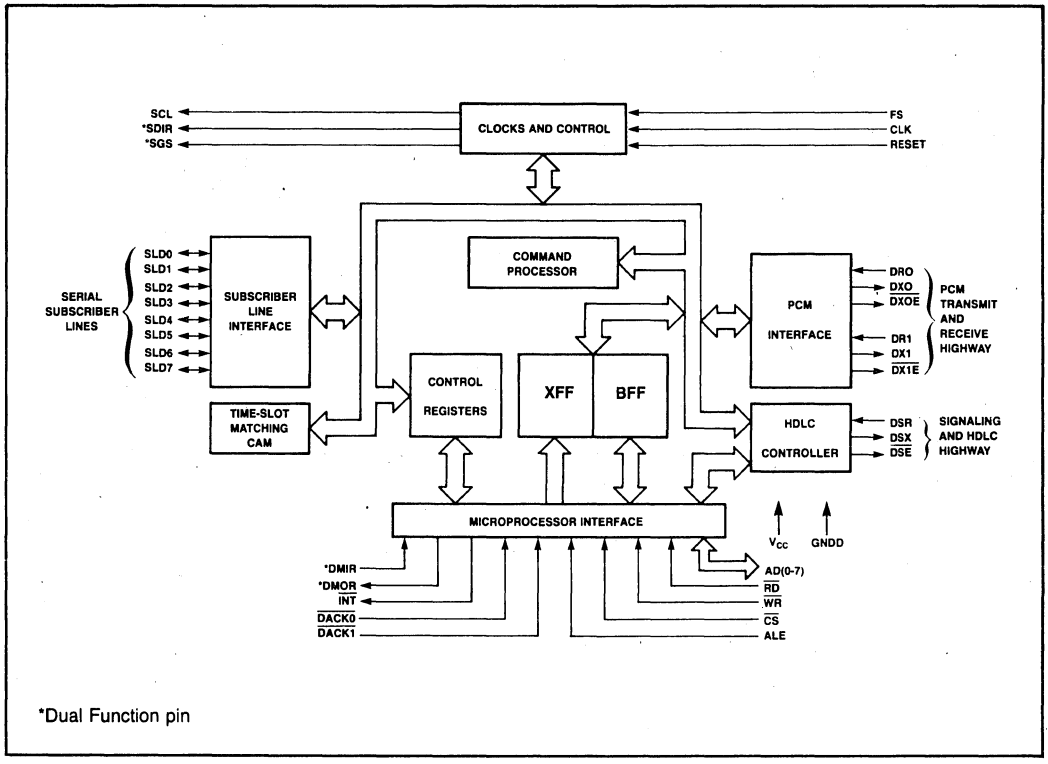

Figure 3. 2952 Block Diagram

The 8031 CPU

The Intel 8031 belongs to the MCS-51 series of single chip microcomputers, and is at the heart of the LCDK, performing control and processing functions for both the primary and secondary stations. The 8031 CPU combines, on a single chip; a 128 x 8 data RAM, 32 input/output lines, two 16-bit timer/event counters, a five source level nested interrupt structure, a programmable serial I/O port; and an on chip oscillator and clock circuits. An 8031 block diagram is shown in Figure 4.

For additional information on the 8031 see the 8051 User's Manual.

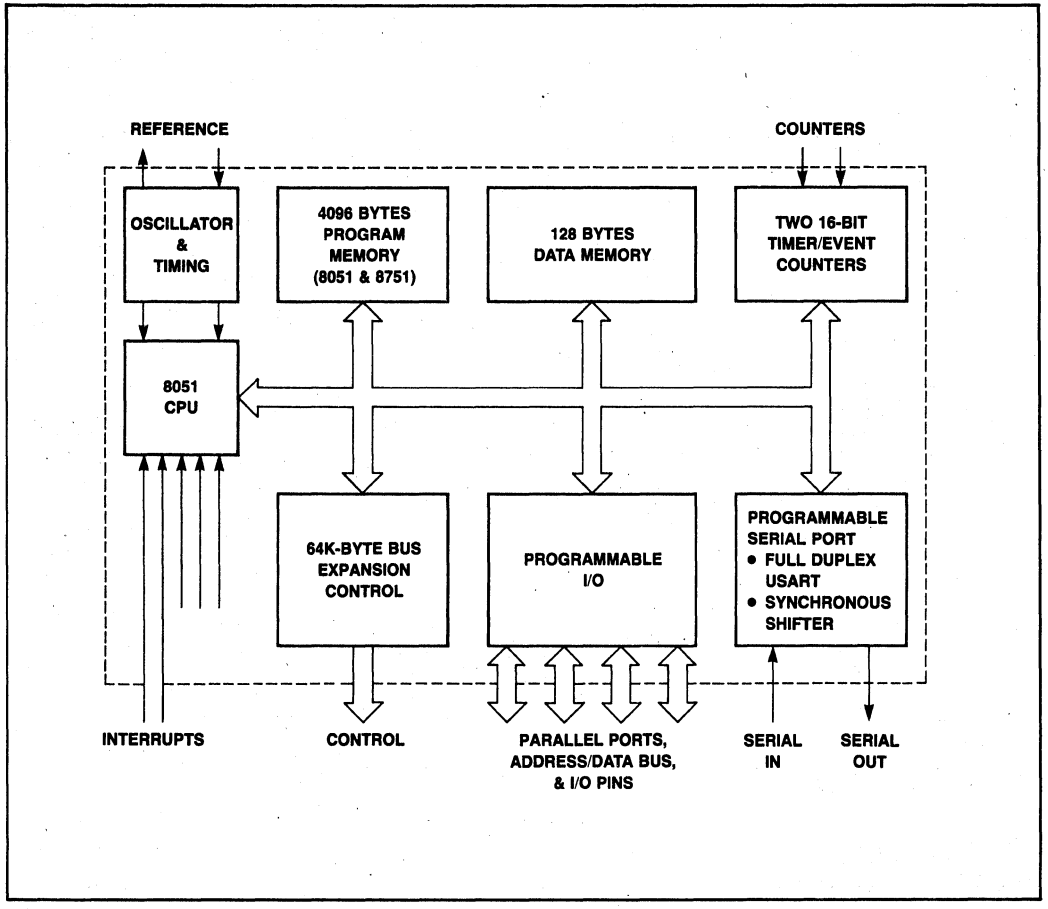

Figure 4. 8031 Block Diagram

System Software

A compact but powerful system monitor is contained in 8K bytes of preprogrammed ROM. The monitor includes system utilities such as command interpretation and interface controls. Table 1 summarizes the LCD-29C51/52 monitor commands.

Table 1

Command	Operation
(LCC reg)	Read or Write a 2952 register.
Half/Full	Half or Full duplex terminal mode.
Help	Displays a Help file.
Byte	Read or Write any external data memory address.
LCC	Relocation of 2952 base address.
GO	Execute user programs resident in memory.

MEMORY

The memory is mapped via 4K byte pages; a maximum of 12K bytes are used allowing a user expansion of memory up to 64K bytes. The memory can be configured as 8K bytes of ROM/PROM plus 2K bytes of RAM or alternatively 12K bytes of ROM/PROM.

USER INTERFACE

Communication with the outside world is accomplished over an RS-232-C compatible link. This serial link will hook up a CRT terminal to the serial port on the 8031. Alternatively an Intellec Development System can be connected to the LCDK, this can now be used as either a dumb terminal or to transport user developed programs to the LCDK, commands for these functions are shown in Table 2. A large area of the board is laid out as general purpose wire-wrap for user custom interface.

Table 2

Command	Operation
DTERM	Places Intellec development system in dumb terminal mode.
Control-D	Transports user developed programs from Intellec development system to the LCDK.

ASSEMBLY

The LCDK-29C51/52 is supplied fully assembled and is ready to go upon power up and terminal connection. The monitor is initialized by twice typing the return key on user terminal.

Documentation

In addition to detailed information on using the monitor, the LCDK-29C51/52 user's manual provides circuit diagrams, a monitor lisitng, and a description of how the system works. The complete design library for the LCDK-29C51/52 is shown in Figure 4 and listed in the specification section under Reference Manuals.

SPECIFICATIONS

Control Processor

Intel 8031 microcomputer.
12MHz clock rate

Memory

ROM — Socket for 256K bytes of program memory, however, a 4K or 2K byte ROM may be inserted.

RAM — Socket for 2K bytes static RAM; user configurable as program or data memory. Alternatively a 4K EPROM such as 2732A may be inserted.

Feature Control Combo

Sockets for four Intel iATC 29C51's.

Line Card Controller

Intel iATC 2952.
User selectable 2.048MHz or 4.096MHz clock rate.

Interface

Ten line ribbon cable for interconnecting the primary and secondary boards, all signals are TTL compatible. Serial RS-232-C compatible interface for a terminal. Terminal baud rate can be 300, 600, 1200, 1800, 2400, 3600 or 4800.

Software

System Monitor — Preprogrammed 2732 ROM.

Monitor I/O — CRT or Intellec Development System.

Physical Characteristics

Width — 12 inch
Height — 1⅝ inch
Depth — 7⅛ inch
Weight — 0.864 lbs.

Mounting

The two board may be:

— plugged into an Intel system rack
— or mounted on five horizontal legs.

Electrical Characteristics

DC Power Requirements

Voltage	Current
±5V ±5% −5V ±5%	2.5A 80mA

Environmental Characteristics

Operating temperature. . . . . .0−50°C